SPECIFICATIONS

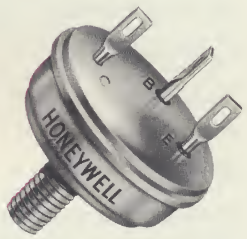
semiconductor products

Minneapolis-Honeywell Regulator Company
MINNEAPOLIS 8, MINNESOTA

2N1157
2N1157A
POWER TRANSISTORS

GERMANIUM PNP ALLOYED JUNCTION POWER TRANSISTORS

- **RELIABILITY**—*Assured* by a proven design; *demonstrated* by time.
- **LOW THERMAL RESISTANCE**—0.4° C/watt junction to heat dissipator surface.
- **HIGH POWER DISSIPATION**—187 watts at T_{MB}=25°C; 75 watts at T_{MB}=70°C.
- **LOW SATURATION VOLTAGE**—0.8 volts at a collector current of 40 amperes.
- **HIGH CURRENT CAPABILITIES**—Typical current gain of 15 at 40 amperes.
- **DOUBLE ENDED PACKAGE**—Simplifies chassis fabrication, assembly and wiring.
- **VERSATILE**—Especially designed for switching, regulator and amplifier applications.



ACTUAL SIZE

DESIGN LIMITS

Junction Temperature, T_J ..... 100°C max.

Thermal Resistance, Junction to Mounting Base, θ_{J-MB} ..... 0.4°C/W max.

Collector-to-Base Voltage, V_{CB}, 2N1157 ..... −60 Vdc max.
2N1157A ..... −80 Vdc max.

Collector-to-Emitter Voltage, V_{CE}
Active Region (Emitter Forward Biased) 2N1157 ..... −45 Vdc max.
2N1157A ..... −50 Vdc max.
Cut-off Region (Emitter Reverse Biased) 2N1157 ..... −60 Vdc max.
2N1157A ..... −80 Vdc max.

Emitter-to-Base Voltage, V_{EB} ..... −28 Vdc max.

Collector Current, I_C ..... −40 Adc max.

Base Current, I_B ..... − 6 Adc max.

PERFORMANCE SPECIFICATIONS, T_{MB} = 25 ± 3° C

Static Characteristics	Conditions	Symbol	Min.	Typ.	Max.	Unit
Current Gain, Common Emitter	V_{CE}=−2V, I_C=−10A −40A*	h_{FE}	38 10	50	84	
Base-to-Emitter Voltage	V_{CE}=−2V, I_C=−10A −40A*	V_{BE}		−0.4	−1.0 −2.0	Vdc
Collector Junction Leakage Current	I_E=0, V_{CB}=−2V −60V −80V**	I_{CBO}		−0.2	−0.7 −7.0 −20	mAdc
Emitter Floating Potential	R_{EB}=10KΩ, V_{CE}=−60V −80V**	V_{EBF}		−0.15	−0.4 −0.5	Vdc
Collector-to-Emitter Voltage (Saturation)	I_C=−40A*, I_B=−6A	V_{CE}(sat)			−0.8	Vdc
Emitter Junction Leakage Current	I_C=0, V_{EB}=−2V V_{EB}=−28V	I_{EBO}		−0.3 −4.0	−1.0 −15	mAdc

Continued on next page

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Supersedes 1 November 1958 Issue

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Semiconductor Products

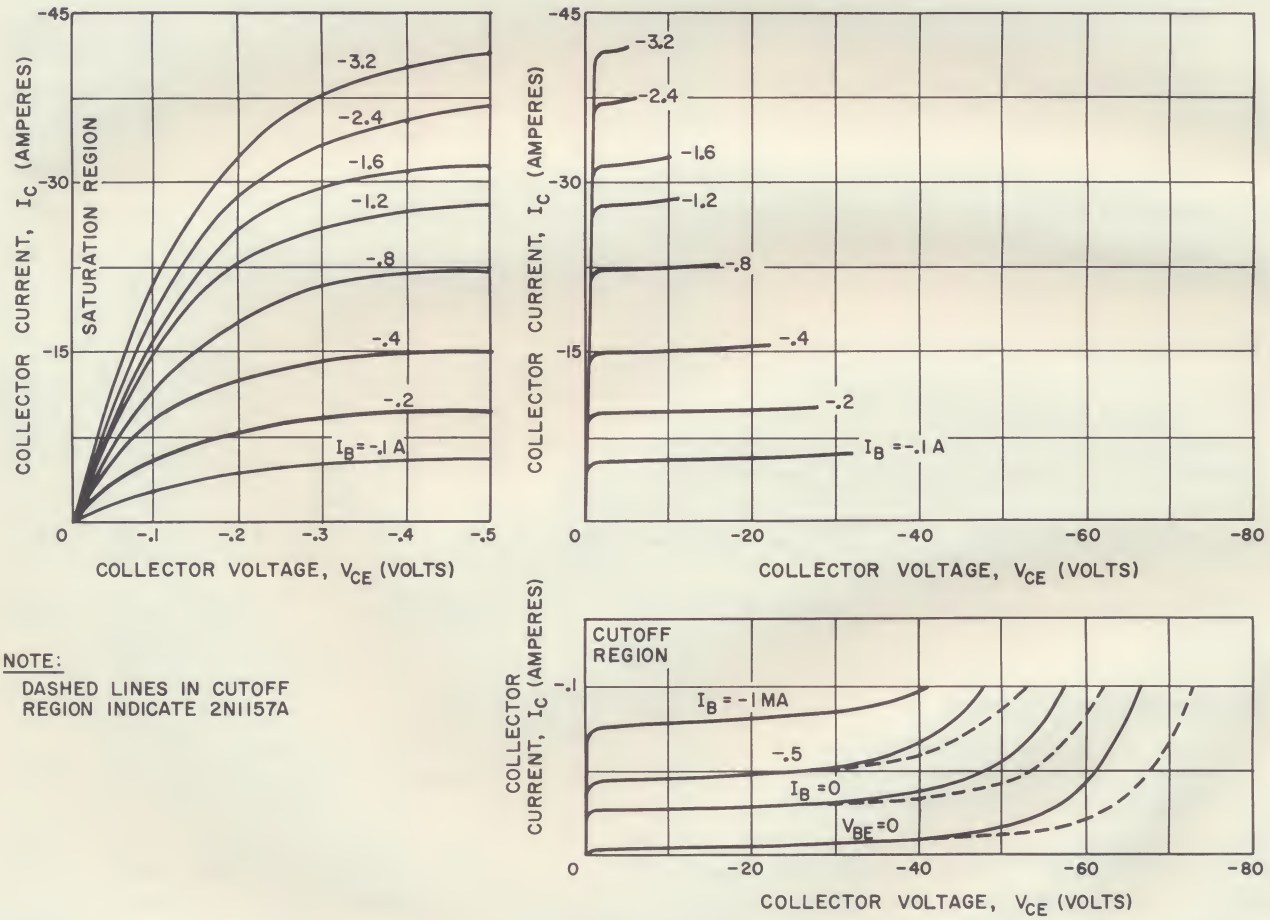
PERFORMANCE SPECIFICATIONS, continued

Dynamic Characteristics	Conditions	Symbol	Min.	Typ.	Max.	Unit
Collector-to-Emitter Voltage	$I_C = -1A$,* $I_B = 0$	V_{CEO}	-45 -50**			V
	$V_{BE} = 0$	V_{CES}	-55 -60**			V
Gain Bandwidth Product	$V_{CE} = -4V$, $I_C = -2A$	$h_{fe} \cdot f_{hfe}$		200		kc
Pulse Rise Time	$I_C = -10A$, $I_B = -1A$	t_r		10		μsec
Pulse Storage Time		t_s		20		μsec
Pulse Fall Time	Test Circuit A	t_f		15		μsec
Thermal Characteristics						
Thermal Resistance***		θ_{J-MB}		0.27	0.4	°C/W
Thermal Time Response		τ	20	60		msec

*To limit collector dissipation use sweep or pulse measurement technique.
**Applies to 2N1157A only.
***Includes dry copper to copper interface between transistor and dissipator.

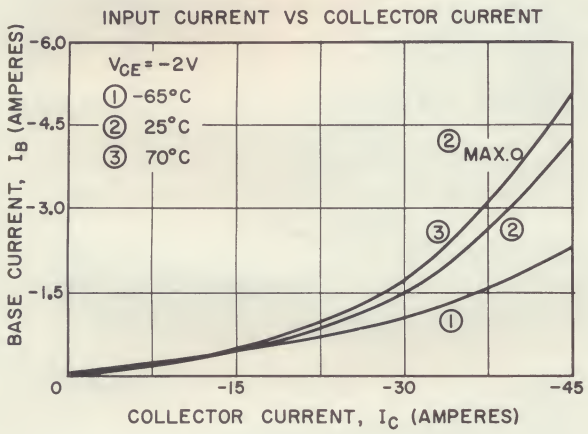
TYPICAL COMMON EMITTER STATIC CHARACTERISTICS $T_{MB} = 25 \pm 3°$ (unless otherwise indicated).

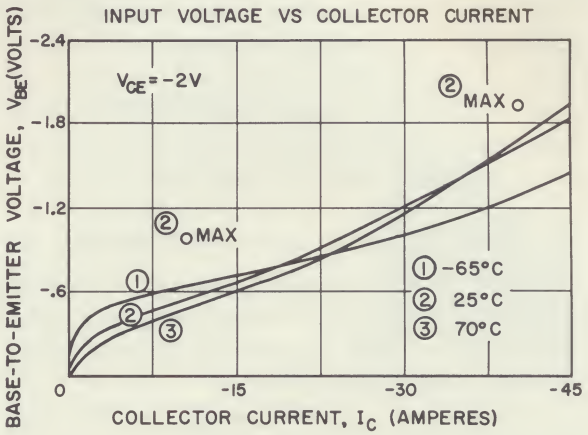
COLLECTOR CHARACTERISTICS

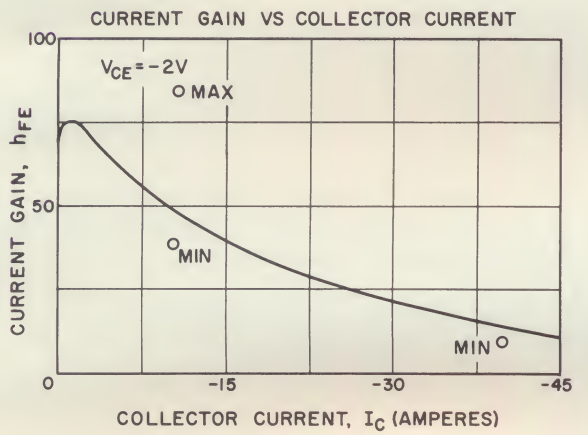


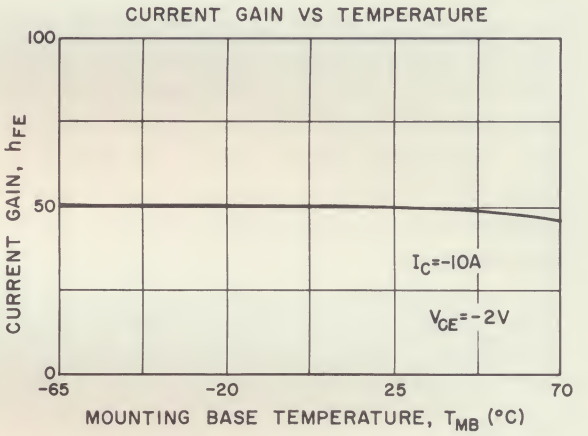
NOTE:
DASHED LINES IN CUTOFF REGION INDICATE 2N1157A

TYPICAL COMMON EMITTER STATIC CHARACTERISTICS—continued

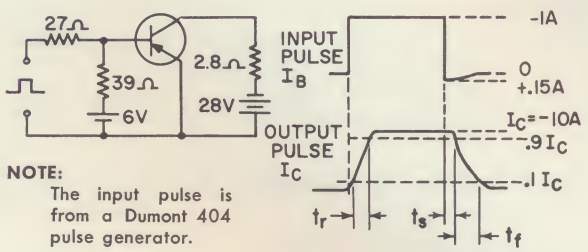








TEST CIRCUIT A—TYPICAL COMMON EMITTER SATURATED SWITCHING RESPONSE



NOTE:
The input pulse is from a Dumont 404 pulse generator.

In common emitter saturated switching circuits, rise time and fall time are dependent in part upon the gain-bandwidth product of the transistor, but can be reduced by application of well known speed-up circuitry techniques.

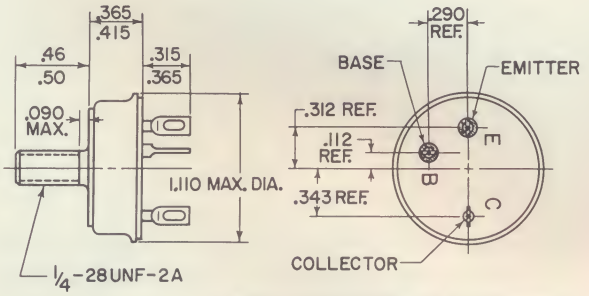
TRANSISTOR MOUNTING

To fully utilize the power dissipating capability of the power transistor, the total thermal resistance, from the power dissipating junctions to the ultimate heat sink, should be kept as low as possible. The internal thermal resistance of this transistor is the lowest in the industry. Proper selection and placement of the heat dissipator will minimize the external thermal resistance. The interface thermal resistance can be minimized by adherence to the following recommendations:

1. The surface on which the transistor is mounted should be flat, smooth, and free from burrs.
2. The surfaces to be joined should be coated with silicone oil.
3. The nut should be tightened to the recommended torque (20 in-lb min., 25 in-lb max.) against a steel washer or the insulating bushing supplied.
4. When the collector must be electrically insulated from the heat dissipator, the mica washer and insulating bushing supplied with the transistor should be used.

The thermal resistance specified for all Honeywell power transistors is based on the temperature gradient from the collector junction to a copper mounting plate. It thus includes a dry copper-to-copper interface.

OUTLINE DIMENSIONS



NOTE: 1. COLLECTOR IS ELECTRICALLY COMMON TO CASE.
2. AVERAGE WEIGHT 0.94 OUNCES.
3. ALL DIMENSIONS IN INCHES.

DETERMINATION OF HEAT DISSIPATOR REQUIREMENTS

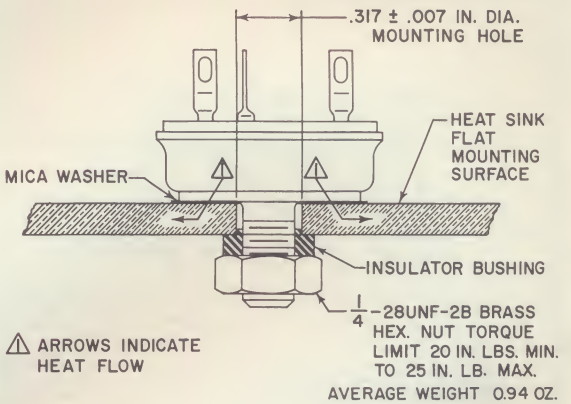
STEADY-STATE CALCULATIONS

The temperature rise from ambient to the junction of the transistor depends on the power dissipated in the transistor and on the total thermal resistance of the heat path from junction to ambient. The total thermal resistance may be conveniently expressed as the sum of the thermal resistance of the transistor, junction to mounting base, θ_T, and the thermal resistance of the heat dissipator to which the transistor is attached, θ_D (θ_D includes the thermal resistance of the mica washer, if used). Therefore, the average temperature rise, ambient to junction, is given by:

$$\Delta T_{J-A} = P_C(\theta_T + \theta_D) \qquad (1)$$

where P_C = average transistor power dissipation.

Since θ_T is fixed for a given transistor, ΔT_{J-A} can be predicted for a given power dissipation and given heat dissipator. Conversely, the required heat dissipator thermal resistance can be predicted, given the power dissipation and the allowable ambient-to-junction temperature rise. Figure 1 establishes this relationship based on the maximum thermal resistance of the transistor specified herein. It is applicable to any type of circuit, steady state or pulsed operation, so long as the average transistor dissipation is known. Care must be exercised in choosing a heat dissipator to insure that it does exhibit the required thermal resistance under the anticipated operating conditions. In general, the thermal resistance of a given heat dissipator changes with temperature and with its orientation.



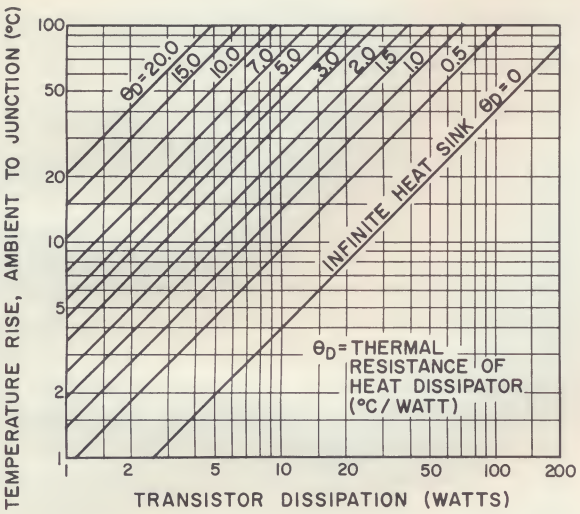


Figure 1

SWITCHING CIRCUIT CALCULATIONS

One of the most common applications of this transistor is in saturated periodic switching circuits, such as solid-state inverters and converters. Operating under these conditions, the maximum instantaneous junction temperature may rise considerably above that predicted on the basis of average dissipation. To determine the maximum junction temperature, it is necessary to take into account the power dissipated during the transient switching interval and to consider the thermal time constant of the transistor. The former is of particular importance in high frequency circuits whereas the latter is of importance in low frequency circuits. Figures 2 and 3, together with the equations given, permit a calculation of maximum junction temperature of the transistor in switching service.

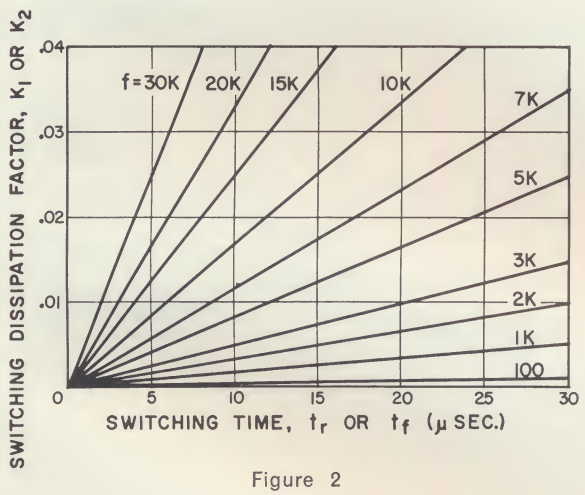


Figure 2

In Figure 2, given the frequency of operation, f, the rise time, t_r, and the fall time, t_f, the two switching dissipation factors, K_1 and K_2, for the turn-on and turn-off transients, respectively, are determined, which when put into Equation (2) yield the average switching transient power dissipation, P_{sw}. It is assumed in Figure 2 that the transistor switches along a resistive load line linearly with respect to time (dv_{CE}/dt = constant and di_C/dt = constant).

$$P_{sw} = (K_1 + K_2) V_{CC} I_m \qquad (2)$$

where V_{CC} = supply voltage
and I_m = maximum collector current.
Equation (3) gives the "on" power dissipation.

$$P_{on} = V_{CE}(sat) I_m \qquad (3)$$

where $V_{CE}(sat)$ = collector-to-emitter saturation voltage.
The "on" dissipation is modified in Equation (4) by the duty cycle, d, and the factor K_3 to account for the thermal time constant of the transistor. K_3 is determined from Figure 3.

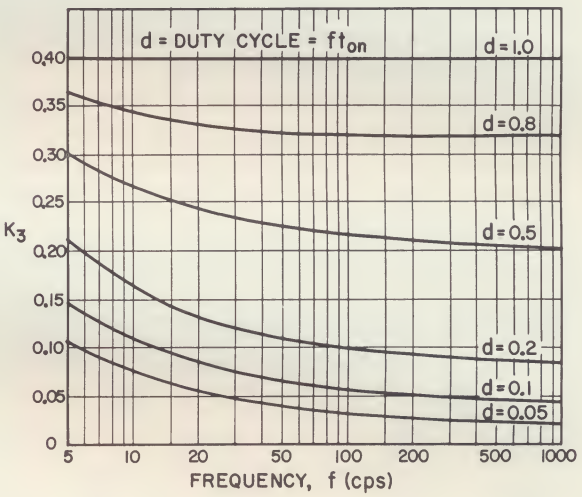


Figure 3

Equation (4) is the complete expression for predicting the maximum junction temperature for a given ambient temperature, T_A, and dissipator thermal resistance, θ_D. It takes into account the time response of junction temperature to the "on" power pulse only. It is assumed that junction temperature does not respond to the maximum instantaneous dissipation during switching because the switching time is very short compared with τ. However, the contribution to junction temperature rise due to the average switching dissipation is included. It is further assumed that the thermal time constant of the heat dissipator used is very long compared with τ and that the "off" dissipation is negligible.

The power dissipated in the base region during the "on" time, $V_{BE}I_B$, has been omitted because its magnitude depends on the degree of overdrive, if employed. If this dissipation becomes significant it should be added to the collector junction dissipation, $V_{CE}(sat)I_m$, in equation (3). However, for most cases equation (3) as given will yield conservative results since the maximum rather than typical transistor thermal resistance has been used in the final equations.

$$T_J(max) = T_A + P_{sw}(\Theta_D + 0.4) + P_{on}(\Theta_D d + K_3) \quad (4)$$

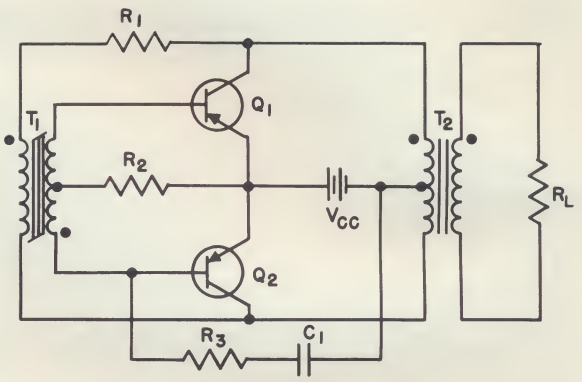
Equation (5) permits the calculation of the required heat dissipator thermal resistance when given the ambient temperature and maximum junction temperature (100°C).

$$\Theta_D = \frac{100°C - T_A - 0.4\,P_{sw} - P_{on}K_3}{P_{sw} + P_{on}d} \quad (5)$$

EXAMPLE

A transistor operates in a solid-state square wave oscillator power inverter as shown in the circuit below. This type of circuit is a typical application of this transistor and is fully described in Honeywell's Application Note AN5A. To permit a calculation of transistor dissipation and junction temperature rise, the following operating conditions are given:

$V_{CC} = 12v$, $V_{CE}(sat) = 0.8v$, $t_r = 15\mu sec.$, $t_f = 20\mu sec.$



$I_m = 40A$, $f = 400cps$, $d = 0.5$, $T_A = 25°C$

FROM FIGURE 2: $K_1 = 0.0015$, $K_2 = 0.0020$
FROM FIGURE 3: $K_3 = 0.21$
BY EQUATION (2): $P_{sw} = (0.0015 + 0.0020) \times 12 \times 40 = 1.68$ watts
BY EQUATION (3): $P_{on} = 0.8 \times 40 = 32$ watts

If the heat dissipator used has a thermal resistance of $\Theta_D = 3.0°C/W$, then the maximum junction temperature by equation (4) is:

$T_J(max) = 25 + 1.68\ (3.0 + 0.4) + 32(3.0 \times 0.5 + 0.21) = 85.4°C$

If it is desired to determine the maximum dissipator thermal resistance permissible for $T_A = 25°C$, equation (5) gives:

$$\Theta_D = \frac{100 - 25 - 0.4 \times 1.68 - 32 \times 0.21}{1.68 + 32 \times 0.5} = 3.8°C/W$$

For additional technical information, prices and quotations for our product, contact the following offices:

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HONEYWELL

SPECIFICATIONS

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MINNEAPOLIS 8, MINNESOTA

2N575
2N575A
POWER TRANSISTORS

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- **RELIABILITY**—*Assured* by a proven design; *demonstrated* by time.
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- **LOW SATURATION VOLTAGE**—0.5 volts at a collector current of 25 amperes.
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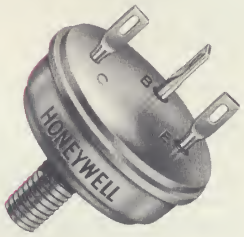

ACTUAL SIZE

DESIGN LIMITS

Junction Temperature, T_J	100°C max.
Thermal Resistance, Junction to Mounting Base, θ_{J-MB}	0.4°C/W max.
Collector-to-Base Voltage, V_{CB}, 2N575	−60 Vdc max.
2N575A	−80 Vdc max.
Collector-to-Emitter Voltage, V_{CE} Active Region (Emitter Forward Biased) 2N575	−50 Vdc max.
2N575A	−55 Vdc max.
Cut-off Region (Emitter Reverse Biased) 2N575	−60 Vdc max.
2N575A	−80 Vdc max.
Emitter-to-Base Voltage, V_{EB}	−28 Vdc max.
Collector Current, I_C	−25 Adc max.
Base Current, I_B	−3.75 Adc max.

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Static Characteristics	Conditions	Symbol	Min.	Typ.	Max.	Unit
Current Gain, Common Emitter	V_{CE}=−2V, I_C=−10A −25A*	h_{FE}	19 10	30	42	
Base-to-Emitter Voltage	V_{CE}=−2V, I_C=−10A −25A*	V_{BE}		−0.6	−1.0 −2.0	Vdc
Collector Junction Leakage Current	I_E=0, V_{CB}=−2V −60V −80V**	I_{CBO}		−0.2	−0.7 −7.0 −20	mAdc
Emitter Floating Potential	R_{EB}=10KΩ, V_{CE}=−60V −80V**	V_{EBF}		−0.15	−0.4 −0.5	Vdc
Collector-to-Emitter Voltage (Saturation)	I_C=−25A*, I_B=−3.75A	V_{CE}(sat)			−0.5	Vdc
Emitter Junction Leakage Current	I_C=0, V_{EB}=−2V V_{EB}=−28V	I_{EBO}		−0.3 −4.0	−1.0 −15	mAdc

Continued on next page

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PERFORMANCE SPECIFICATIONS, continued

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	$V_{BE} = 0$	V_{CES}	-55 -65**			V
Gain Bandwidth Product	$V_{CE} = -4V$, $I_C = -2A$	$h_{fe} \cdot f_{hfe}$		150		kc
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Thermal Time Response		τ	20	60		msec

*To limit collector dissipation use sweep or pulse measurement technique.
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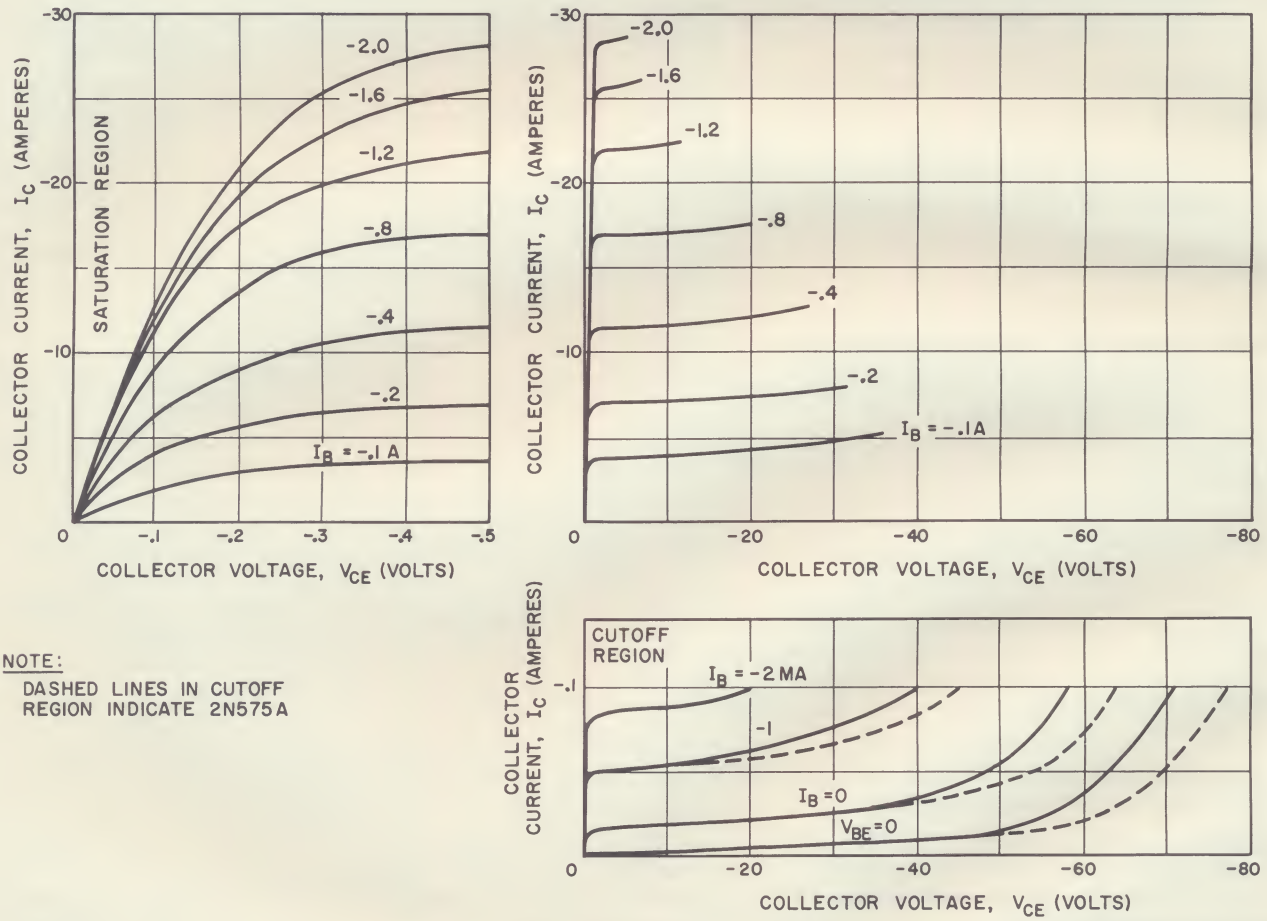
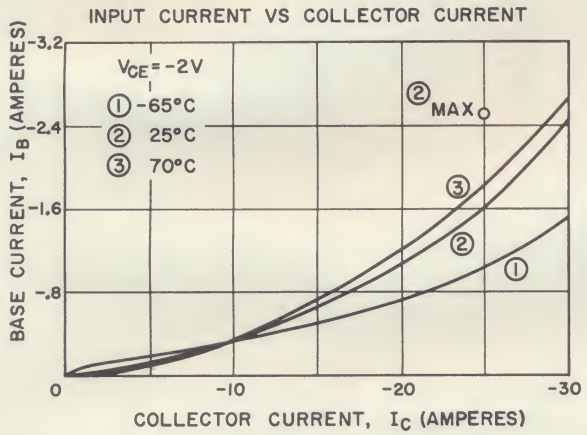
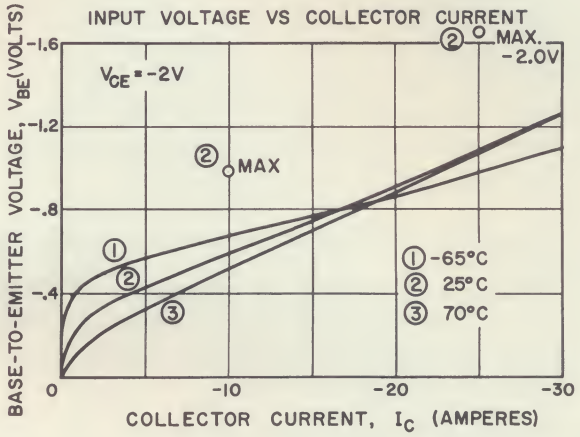
COLLECTOR CHARACTERISTICS

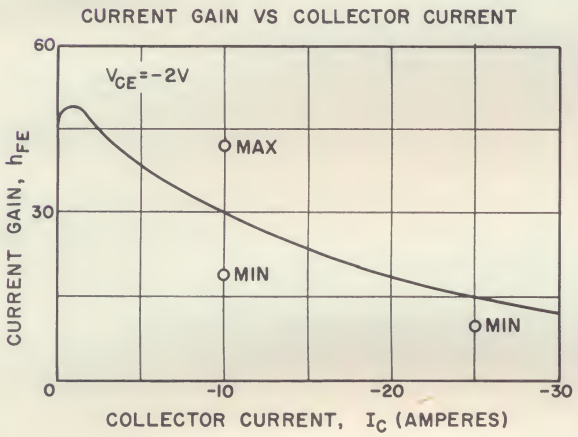


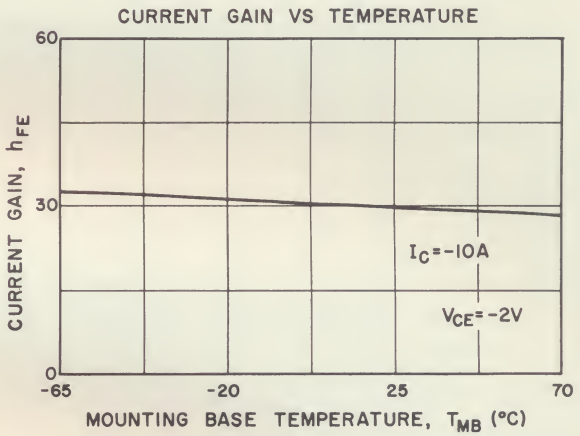
NOTE:
DASHED LINES IN CUTOFF REGION INDICATE 2N575A

TYPICAL COMMON EMITTER STATIC CHARACTERISTICS—continued

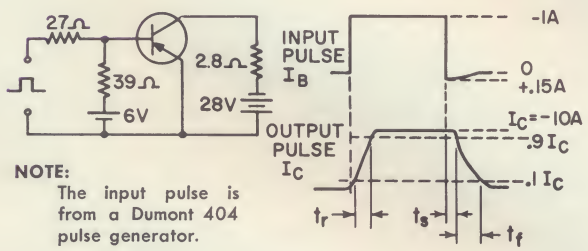








TEST CIRCUIT A—TYPICAL COMMON EMITTER SATURATED SWITCHING RESPONSE



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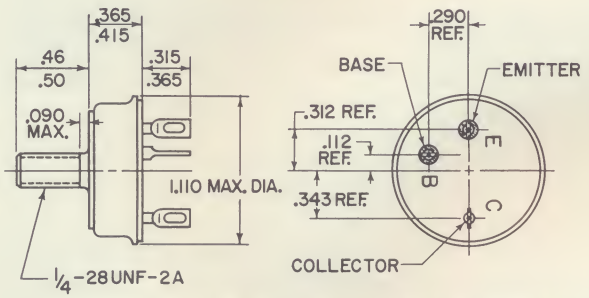
OUTLINE DIMENSIONS



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2. AVERAGE WEIGHT 0.94 OUNCES.
3. ALL DIMENSIONS IN INCHES.

DETERMINATION OF HEAT DISSIPATOR REQUIREMENTS

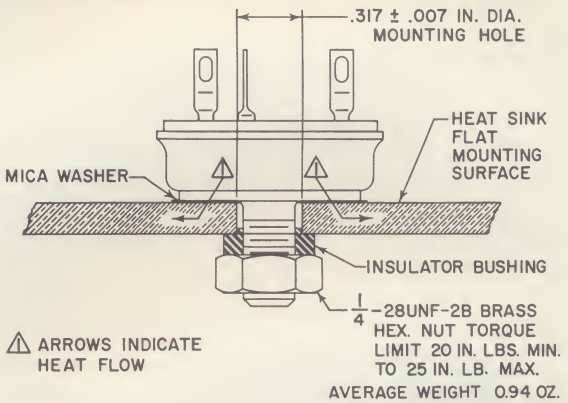
STEADY-STATE CALCULATIONS

The temperature rise from ambient to the junction of the transistor depends on the power dissipated in the transistor and on the total thermal resistance of the heat path from junction to ambient. The total thermal resistance may be conveniently expressed as the sum of the thermal resistance of the transistor, junction to mounting base, Θ_T, and the thermal resistance of the heat dissipator to which the transistor is attached, Θ_D (Θ_D includes the thermal resistance of the mica washer, if used). Therefore, the average temperature rise, ambient to junction, is given by:

$$\Delta T_{J-A} = P_C(\Theta_T + \Theta_D) \qquad (1)$$

where P_C = average transistor power dissipation.

Since Θ_T is fixed for a given transistor, ΔT_{J-A} can be predicted for a given power dissipation and given heat dissipator. Conversely, the required heat dissipator thermal resistance can be predicted, given the power dissipation and the allowable ambient-to-junction temperature rise. Figure 1 establishes this relationship based on the maximum thermal resistance of the transistor specified herein. It is applicable to any type of circuit, steady state or pulsed operation, so long as the average transistor dissipation is known. Care must be exercised in choosing a heat dissipator to insure that it does exhibit the required thermal resistance under the anticipated operating conditions. In general, the thermal resistance of a given heat dissipator changes with temperature and with its orientation.



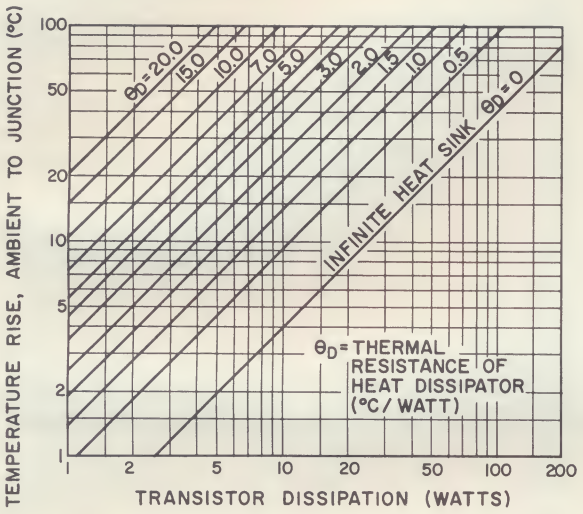


Figure 1

SWITCHING CIRCUIT CALCULATIONS

One of the most common applications of this transistor is in saturated periodic switching circuits, such as solid-state inverters and converters. Operating under these conditions, the maximum instantaneous junction temperature may rise considerably above that predicted on the basis of average dissipation. To determine the maximum junction temperature, it is necessary to take into account the power dissipated during the transient switching interval and to consider the thermal time constant of the transistor. The former is of particular importance in high frequency circuits whereas the latter is of importance in low frequency circuits. Figures 2 and 3, together with the equations given, permit a calculation of maximum junction temperature of the transistor in switching service.

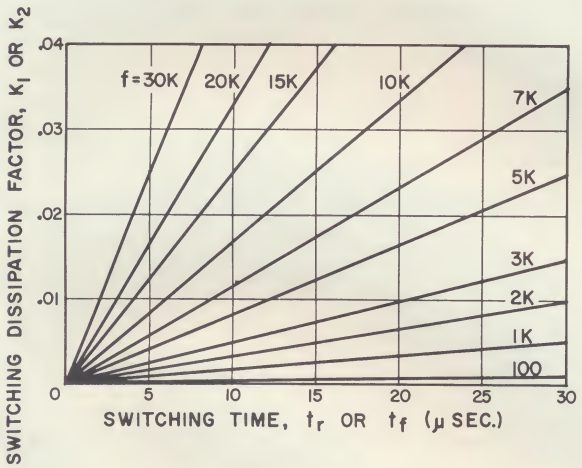


Figure 2

In Figure 2, given the frequency of operation, f, the rise time, t_r, and the fall time, t_f, the two switching dissipation factors, K_1 and K_2, for the turn-on and turn-off transients, respectively, are determined, which when put into Equation (2) yield the average switching transient power dissipation, P_{sw}. It is assumed in Figure 2 that the transistor switches along a resistive load line linearly with respect to time (dv_{CE}/dt = constant and di_C/dt = constant).

$$P_{sw} = (K_1 + K_2) V_{CC} I_m \qquad (2)$$

where V_{CC} = supply voltage
and I_m = maximum collector current.
Equation (3) gives the "on" power dissipation.

$$P_{on} = V_{CE}(sat) I_m \qquad (3)$$

where $V_{CE}(sat)$ = collector-to-emitter saturation voltage.
The "on" dissipation is modified in Equation (4) by the duty cycle, d, and the factor K_3 to account for the thermal time constant of the transistor. K_3 is determined from Figure 3.

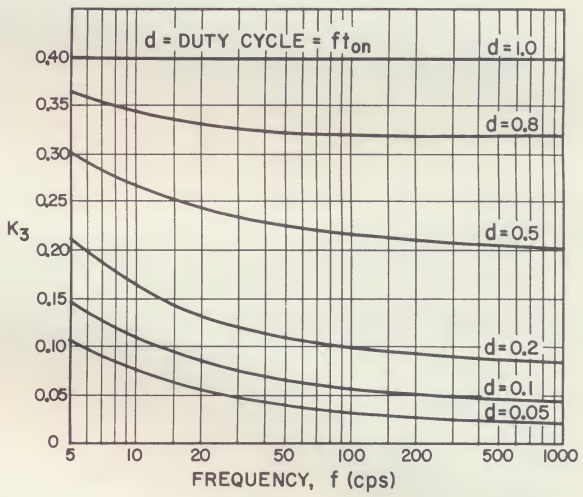


Figure 3

Equation (4) is the complete expression for predicting the maximum junction temperature for a given ambient temperature, T_A, and dissipator thermal resistance, θ_D. It takes into account the time response of junction temperature to the "on" power pulse only. It is assumed that junction temperature does not respond to the maximum instantaneous dissipation during switching because the switching time is very short compared with τ. However, the contribution to junction temperature rise due to the average switching dissipation is included. It is further assumed that the thermal time constant of the heat dissipator used is very long compared with τ and that the "off" dissipation is negligible.

The power dissipated in the base region during the "on" time, $V_{BE}I_B$, has been omitted because its magnitude depends on the degree of overdrive, if employed. If this dissipation becomes significant it should be added to the collector junction dissipation, $V_{CE}(sat)I_m$, in equation (3). However, for most cases equation (3) as given will yield conservative results since the maximum rather than typical transistor thermal resistance has been used in the final equations.

$$T_J(max)=T_A+P_{sw}(\Theta_D+0.4)+P_{on}(\Theta_D d+K_3) \quad (4)$$

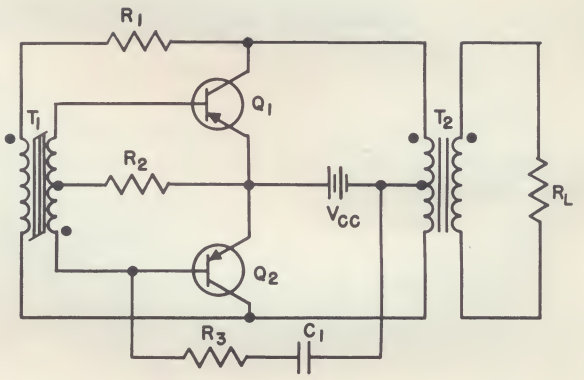
Equation (5) permits the calculation of the required heat dissipator thermal resistance when given the ambient temperature and maximum junction temperature (100°C).

$$\Theta_D=\frac{100°C-T_A-0.4\,P_{sw}-P_{on}K_3}{P_{sw}+P_{on}d} \quad (5)$$

EXAMPLE

A transistor operates in a solid-state square wave oscillator power inverter as shown in the circuit below. This type of circuit is a typical application of this transistor and is fully described in Honeywell's Application Note AN5A. To permit a calculation of transistor dissipation and junction temperature rise, the following operating conditions are given:

$V_{CC}=12v$, $V_{CE}(sat)=0.5v$, $t_r=10\mu sec.$, $t_f=15\mu sec.$



$I_m=25A$, $f=5000cps$, $d=0.5$, $T_A=25°C$

FROM FIGURE 2: $K_1=0.0083$, $K_2=0.0125$
FROM FIGURE 3: $K_3=0.2$
BY EQUATION (2): $P_{sw}=(0.0083+0.0125)\times 12\times 25=6.24$ watts
BY EQUATION (3): $P_{on}=0.5\times 25=12.5$ watts

If the heat dissipator used has a thermal resistance of $\Theta_D=3.0°C/W$, then the maximum junction temperature by equation (4) is:

$T_J(max)=25+6.24(3.0+0.4)+12.5(3.0\times0.5+0.2)=67.5°C$

If it is desired to determine the maximum dissipator thermal resistance permissible for $T_A=25°C$, equation (5) gives:

$$\Theta_D=\frac{100-25-0.4\times 6.24-12.5\times 0.2}{6.24+12.5\times 0.5}=5.6°C/W$$

For additional technical information, prices and quotations for our product, contact the following offices:

GENERAL SALES OFFICE
1015 South Sixth Street
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LOS ANGELES 22, CALIFORNIA
6620 Telegraph Road
Tel. RAymond 3-6611

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Tel. CHerry 1-2310

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HONEYWELL

SPECIFICATIONS

semiconductor products

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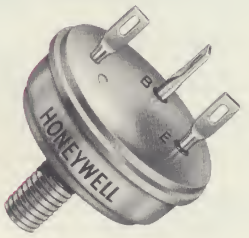
2N574
2N574A
POWER TRANSISTORS

GERMANIUM PNP ALLOYED JUNCTION POWER TRANSISTORS

- **RELIABILITY**—*Assured* by a proven design; *demonstrated* by time.
- **LOW THERMAL RESISTANCE**—0.4° C/watt junction to heat dissipator surface.
- **HIGH POWER DISSIPATION**—187 watts at T_{MB}=25°C; 75 watts at T_{MB}=70°C.
- **LOW SATURATION VOLTAGE**—0.2 volts at a collector current of 10 amperes.
- **HIGH CURRENT CAPABILITIES**—Typical current gain of 15 at 10 amperes.
- **DOUBLE ENDED PACKAGE**—Simplifies chassis fabrication, assembly and wiring.
- **VERSATILE**—Especially designed for switching, regulator and amplifier applications.



ACTUAL SIZE

DESIGN LIMITS

Junction Temperature, T_J	100°C max.
Thermal Resistance, Junction to Mounting Base, θ_{J-MB}	0.4°C/W max.
Collector-to-Base Voltage, V_{CB}, 2N574	−60 Vdc max.
2N574A	−80 Vdc max.
Collector-to-Emitter Voltage, V_{CE}	
Active Region (Emitter Forward Biased) 2N574	−55 Vdc max.
2N574A	−60 Vdc max.
Cut-off Region (Emitter Reverse Biased) 2N574	−60 Vdc max.
2N574A	−80 Vdc max.
Emitter-to-Base Voltage, V_{EB}	−28 Vdc max.
Collector Current, I_C	−10 Adc max.
Base Current, I_B	− 2 Adc max.

PERFORMANCE SPECIFICATIONS, T_{MB} = 25 ± 3° C

Static Characteristics	Conditions	Symbol	Min.	Typ.	Max.	Unit
Current Gain, Common Emitter	V_{CE}=−2V, I_C=−10A	h_{FE}	9	15	22	
Base-to-Emitter Voltage	V_{CE}=−2V, I_C=−10A	V_{BE}		−0.8	−1.0	Vdc
Collector Junction Leakage Current	I_E=0, V_{CB}=−2V	I_{CBO}		−0.2	−0.7	mAdc
	−60V				−7.0	
	−80V*				−20	
Emitter Floating Potential	R_{EB}=10KΩ, V_{CE}=−60V	V_{EBF}		−0.15	−0.4	Vdc
	−80V*				−0.5	
Collector-to-Emitter Voltage (Saturation)	I_C=−10A, I_B=−2A	V_{CE}(sat)			−0.2	Vdc
Emitter Junction Leakage Current	I_C=0, V_{EB}=−2V	I_{EBO}		−0.3	−1.0	mAdc
	V_{EB}=−28V			−4.0	−15	

Continued on next page

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Honeywell

Semiconductor Products

PERFORMANCE SPECIFICATIONS, continued

Dynamic Characteristics	Conditions	Symbol	Min.	Typ.	Max.	Unit
Collector-to-Emitter Voltage	$I_C = -1A$,** $I_B = 0$	V_{CEO}	-55 -60*			V
	$V_{BE} = 0$	V_{CES}	-55 -70*			V
Gain Bandwidth Product	$V_{CE} = -4V$, $I_C = -2A$	$h_{fe} \cdot f_{hfe}$		100		kc
Pulse Rise Time	$I_C = -10A$, $I_B = -1A$	t_r		20		μsec
Pulse Storage Time		t_s		10		μsec
Pulse Fall Time	Test Circuit A	t_f		25		μsec
Thermal Characteristics						
Thermal Resistance***		θ_{J-MB}		0.27	0.4	°C/W
Thermal Time Response		τ	20	60		msec

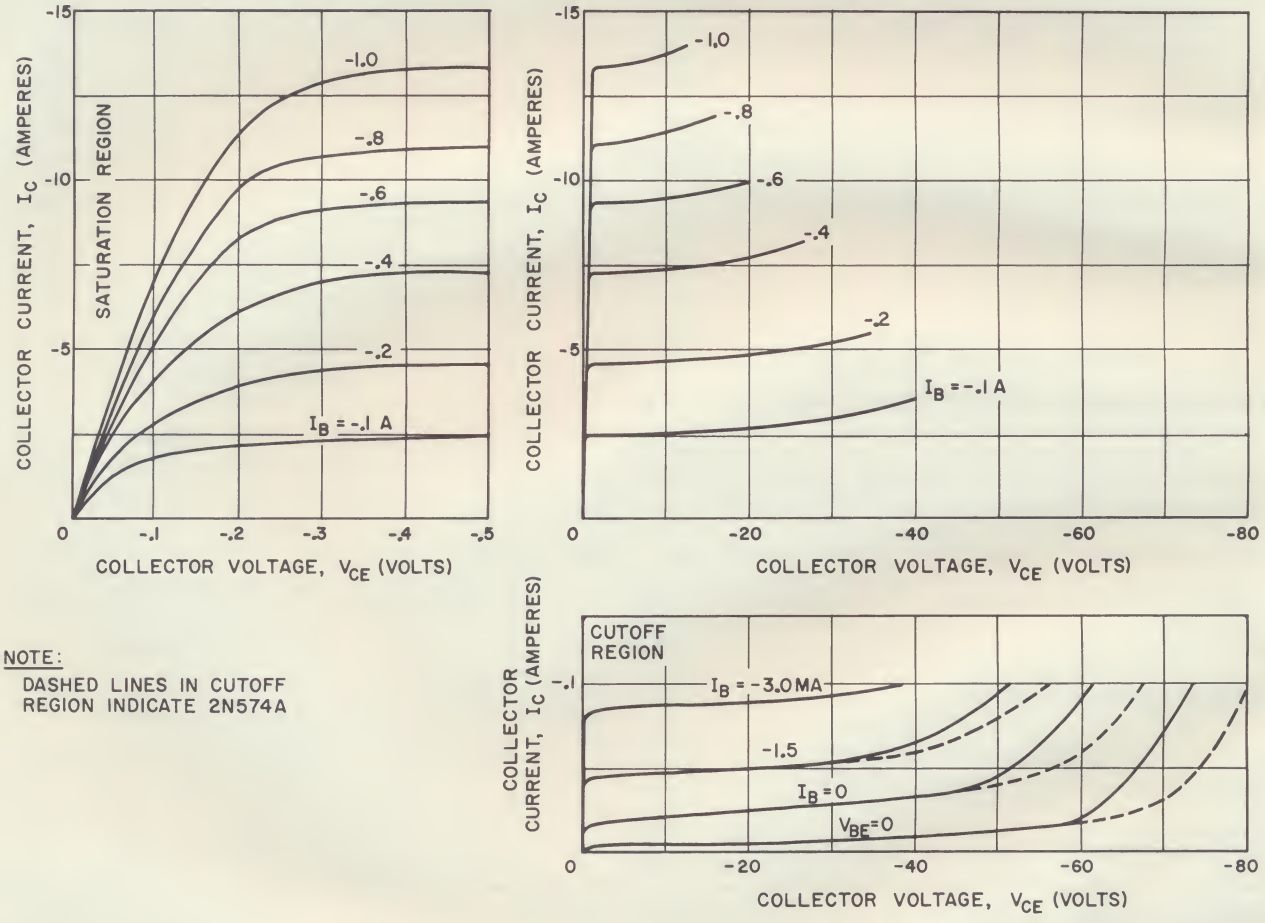
*Applies to 2N574A only.

**To limit collector dissipation use sweep or pulse measurement technique.

***Includes dry copper to copper interface between transistor and dissipator.

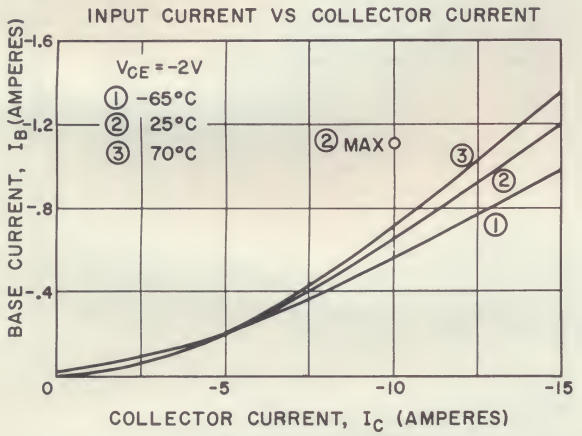
TYPICAL COMMON EMITTER STATIC CHARACTERISTICS $T_{MB} = 25 \pm 3°$ (unless otherwise indicated).

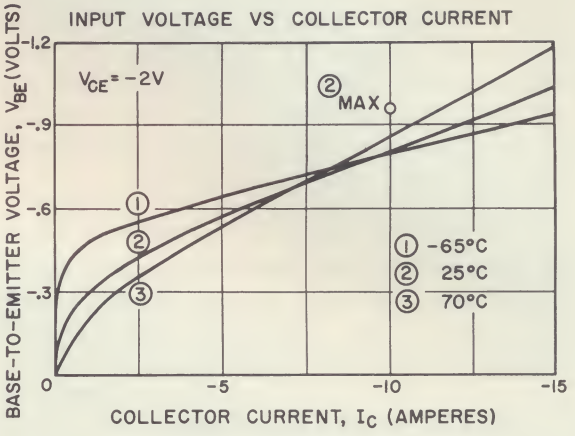
COLLECTOR CHARACTERISTICS

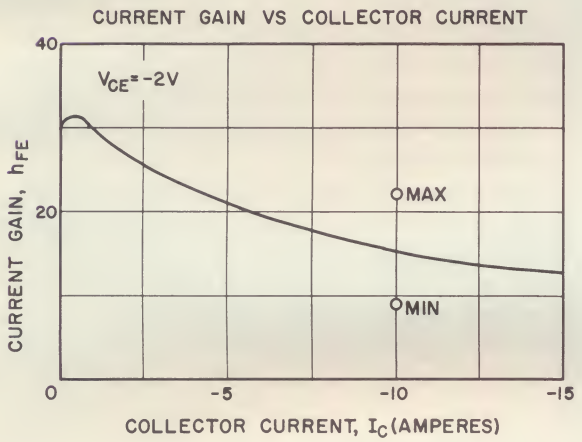


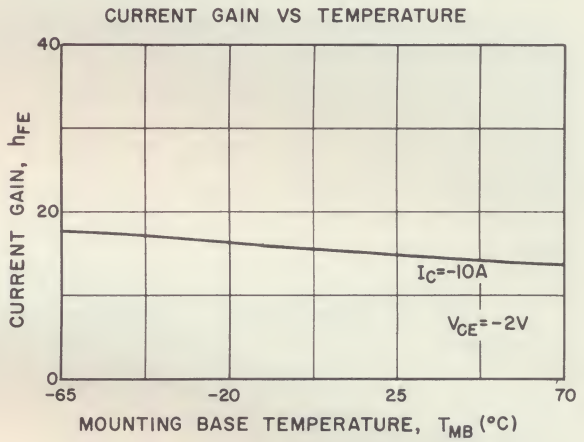
NOTE:
DASHED LINES IN CUTOFF REGION INDICATE 2N574A

TYPICAL COMMON EMITTER STATIC CHARACTERISTICS—continued

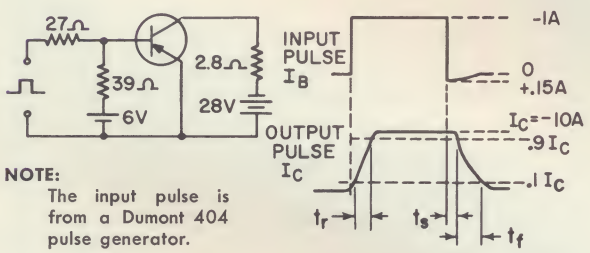








TEST CIRCUIT A—TYPICAL COMMON EMITTER SATURATED SWITCHING RESPONSE



NOTE:
The input pulse is from a Dumont 404 pulse generator.

In common emitter saturated switching circuits, rise time and fall time are dependent in part upon the gain-bandwidth product of the transistor, but can be reduced by application of well known speed-up circuitry techniques.

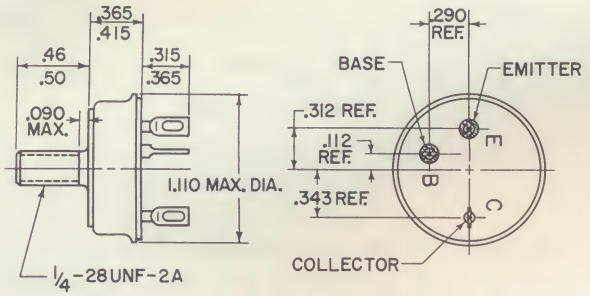
TRANSISTOR MOUNTING

To fully utilize the power dissipating capability of the power transistor, the total thermal resistance, from the power dissipating junctions to the ultimate heat sink, should be kept as low as possible. The internal thermal resistance of this transistor is the lowest in the industry. Proper selection and placement of the heat dissipator will minimize the external thermal resistance. The interface thermal resistance can be minimized by adherence to the following recommendations:

1. The surface on which the transistor is mounted should be flat, smooth, and free from burrs.
2. The surfaces to be joined should be coated with silicone oil.
3. The nut should be tightened to the recommended torque (20 in-lb min., 25 in-lb max.) against a steel washer or the insulating bushing supplied.
4. When the collector must be electrically insulated from the heat dissipator, the mica washer and insulating bushing supplied with the transistor should be used.

The thermal resistance specified for all Honeywell power transistors is based on the temperature gradient from the collector junction to a copper mounting plate. It thus includes a dry copper-to-copper interface.

OUTLINE DIMENSIONS



NOTE: 1. COLLECTOR IS ELECTRICALLY COMMON TO CASE.
2. AVERAGE WEIGHT 0.94 OUNCES.
3. ALL DIMENSIONS IN INCHES.

DETERMINATION OF HEAT DISSIPATOR REQUIREMENTS

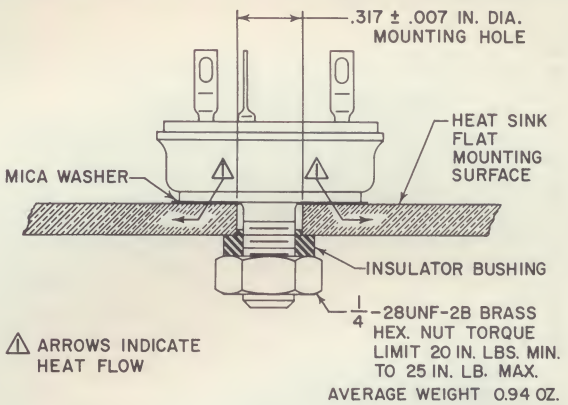
STEADY-STATE CALCULATIONS

The temperature rise from ambient to the junction of the transistor depends on the power dissipated in the transistor and on the total thermal resistance of the heat path from junction to ambient. The total thermal resistance may be conveniently expressed as the sum of the thermal resistance of the transistor, junction to mounting base, θ_T, and the thermal resistance of the heat dissipator to which the transistor is attached, θ_D (θ_D includes the thermal resistance of the mica washer, if used). Therefore, the average temperature rise, ambient to junction, is given by:

$$\Delta T_{J-A} = P_C(\theta_T + \theta_D) \qquad (1)$$

where P_C = average transistor power dissipation.

Since θ_T is fixed for a given transistor, ΔT_{J-A} can be predicted for a given power dissipation and given heat dissipator. Conversely, the required heat dissipator thermal resistance can be predicted, given the power dissipation and the allowable ambient-to-junction temperature rise. Figure 1 establishes this relationship based on the maximum thermal resistance of the transistor specified herein. It is applicable to any type of circuit, steady state or pulsed operation, so long as the average transistor dissipation is known. Care must be exercised in choosing a heat dissipator to insure that it does exhibit the required thermal resistance under the anticipated operating conditions. In general, the thermal resistance of a given heat dissipator changes with temperature and with its orientation.



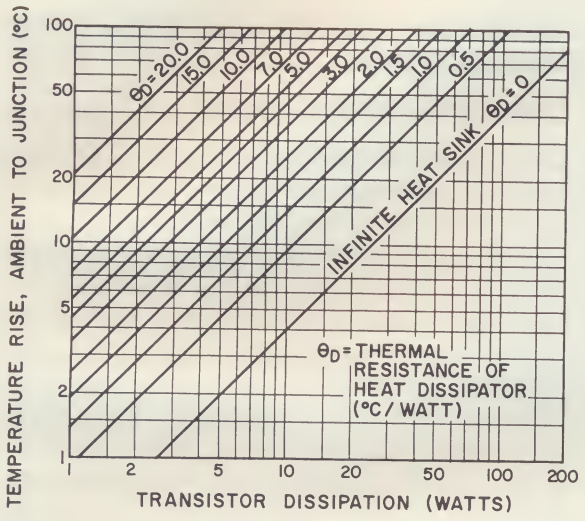


Figure 1

SWITCHING CIRCUIT CALCULATIONS

One of the most common applications of this transistor is in saturated periodic switching circuits, such as solid-state inverters and converters. Operating under these conditions, the maximum instantaneous junction temperature may rise considerably above that predicted on the basis of average dissipation. To determine the maximum junction temperature, it is necessary to take into account the power dissipated during the transient switching interval and to consider the thermal time constant of the transistor. The former is of particular importance in high frequency circuits whereas the latter is of importance in low frequency circuits. Figures 2 and 3, together with the equations given, permit a calculation of maximum junction temperature of the transistor in switching service.

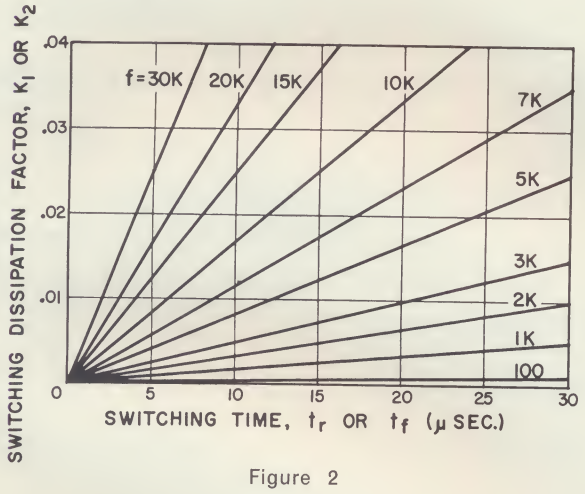


Figure 2

In Figure 2, given the frequency of operation, f, the rise time, t_r, and the fall time, t_f, the two switching dissipation factors, K_1 and K_2, for the turn-on and turn-off transients, respectively, are determined, which when put into Equation (2) yield the average switching transient power dissipation, P_{sw}. It is assumed in Figure 2 that the transistor switches along a resistive load line linearly with respect to time (dv_{CE}/dt = constant and di_C/dt = constant).

$$P_{sw} = (K_1 + K_2) V_{CC} I_m \qquad (2)$$

where V_{CC} = supply voltage
and I_m = maximum collector current.
Equation (3) gives the "on" power dissipation.

$$P_{on} = V_{CE}(sat) I_m \qquad (3)$$

where $V_{CE}(sat)$ = collector-to-emitter saturation voltage.
The "on" dissipation is modified in Equation (4) by the duty cycle, d, and the factor K_3 to account for the thermal time constant of the transistor. K_3 is determined from Figure 3.

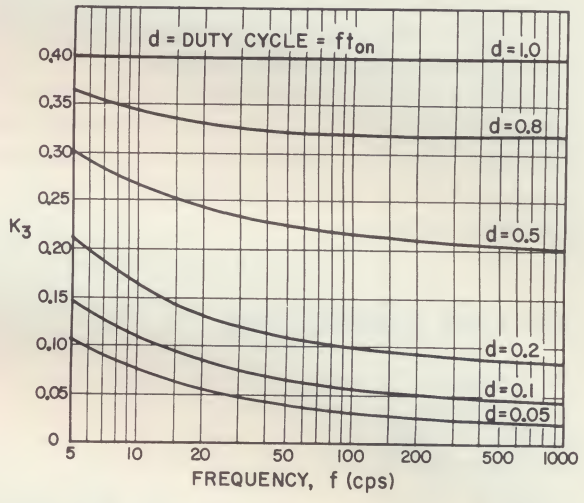


Figure 3

Equation (4) is the complete expression for predicting the maximum junction temperature for a given ambient temperature, T_A, and dissipator thermal resistance, θ_D. It takes into account the time response of junction temperature to the "on" power pulse only. It is assumed that junction temperature does not respond to the maximum instantaneous dissipation during switching because the switching time is very short compared with τ. However, the contribution to junction temperature rise due to the average switching dissipation is included. It is further assumed that the thermal time constant of the heat dissipator used is very long compared with τ and that the "off" dissipation is negligible.

The power dissipated in the base region during the "on" time, $V_{BE}I_B$, has been omitted because its magnitude depends on the degree of overdrive, if employed. If this dissipation becomes significant it should be added to the collector junction dissipation, $V_{CE}(sat)I_m$, in equation (3). However, for most cases equation (3) as given will yield conservative results since the maximum rather than typical transistor thermal resistance has been used in the final equations.

$$T_J(max) = T_A + P_{sw}(\theta_D + 0.4) + P_{on}(\theta_D d + K_3) \quad (4)$$

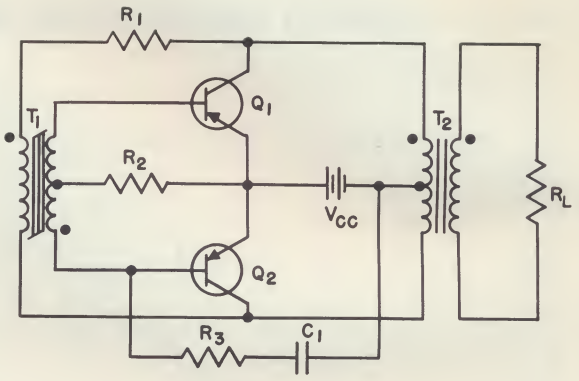
Equation (5) permits the calculation of the required heat dissipator thermal resistance when given the ambient temperature and maximum junction temperature (100°C).

$$\theta_D = \frac{100°C - T_A - 0.4\ P_{sw} - P_{on}K_3}{P_{sw} + P_{on}d} \quad (5)$$

EXAMPLE

A transistor operates in a solid-state square wave oscillator power inverter as shown in the circuit below. This type of circuit is a typical application of this transistor and is fully described in Honeywell's Application Note AN5A. To permit a calculation of transistor dissipation and junction temperature rise, the following operating conditions are given:

$V_{CC} = 28v$, $V_{CE}(sat) = 0.2v$, $t_r = 20\mu sec.$, $t_f = 25\mu sec.$



$I_m = 10A$, $f = 1000cps$, $d = 0.5$, $T_A = 25°C$

FROM FIGURE 2: $K_1 = 0.0033$, $K_2 = 0.0042$
FROM FIGURE 3: $K_3 = 0.20$
BY EQUATION (2): $P_{sw} = (0.0033 + 0.0042) \times 28 \times 10 = 2.10$ watts
BY EQUATION (3): $P_{on} = 0.2 \times 10 = 2.0$ watts

If the heat dissipator used has the thermal resistance of $\theta_D = 3.0°C/W$, then the maximum junction temperature by equation (4) is:

$T_J(max.) = 25 + 2.10\ (3.0 + 0.4) + 2.0\ (3.0 \times 0.5 + 0.20) = 35.5°C$

If it is desired to determine the maximum dissipator thermal resistance permissible for $T_A = 25°C$, equation (5) gives:

$$\theta_D = \frac{100 - 25 - 0.4 \times 2.10 - 2.0 \times .2}{2.10 + 2.0 \times 0.5} = 23.8°C/W$$

HONEYWELL

SPECIFICATIONS

semiconductor products

Minneapolis-Honeywell Regulator Company

MINNEAPOLIS 8, MINNESOTA

2N539† 2N539A†

POWER TRANSISTORS

GENERAL INFORMATION

The Honeywell 2N539 is a rugged, hermetically sealed germanium PNP transistor designed for a variety of uses including servo amplifiers, power conversion, voltage regulation, switching, etc. It is capable of carrying currents in excess of 3 amperes and of dissipating 10 watts of power at a case temperature of 71°C. *It is dynamically tested to insure 80-volt collector diode and reach through (punch through) ratings and a 55-volt $\alpha = 1$ rating.* Limits of current gain and transconductance are the same as those for the former Honeywell type H6. The exact replacement for the H6, however, is the 2N539A which is unilaterally interchangeable with the 2N539 but, in addition, is characterized by power conductance and input resistance limits.

ACTUAL SIZE

DESIGN LIMITS

Junction Temperature, T_J	100° C max.
Thermal Resistance, Junctions to Mounting Base, θ	2.2° C/W. max.
Collector-to-Base Voltage, V_{CB}	−80 Vdc max.
Collector-to-Emitter Voltage, V_{CE}	
Active Region (Emitter Forward Biased)	−55 Vdc max.
Cutoff Region (Emitter Reverse Biased)	−80 Vdc max.
Emitter-to-Base Voltage, V_{EB}	−28 Vdc max.
Emitter Current, I_E	−3.5 Adc max.
Base Current, I_B	−0.5 Adc max.

PERFORMANCE SPECIFICATIONS, $T_{MB} = 25° \pm 3°C$ (±3% tolerance applies to all electrical measurements)

Characteristic	Conditions	Symbol	Min.	Typ.	Max.	Unit
Current Gain, Common Emitter	$I_C = -2a$, $V_{CE} = -2v$	h_{FE}	30	43	75	
Base-to-Emitter Voltage	$I_C = -2a$, $V_{CE} = -2v$	V_{BE}	−1.0	−1.7	−2.5	Vdc
*Power Conductance, Common Emitter	$I_C = -2a$, $V_{CE} = -2v$	G_P	35	51	105	mho
*Input Resistance, Common Emitter	$I_C = -2a$, $V_{CE} = -2v$	H_{IE}	27	37	54	ohm
Thermal Resistance, Junctions to Mounting Base		θ		1.7	2.2	
Time Response of Junction Temperature		τ	10	30		msec.
Collector Junction Leakage Current	$I_E = 0$, $V_{CB} = -2v$ $-28v$ $-80v$	I_{CBO}		−0.04 −0.1	−0.1 −1.0 −2.0	mAdc
Alpha = 1 Voltage, Collector Junction	(See Reverse Side)	$V_{\alpha=1}$	−55			Vdc
Emitter Floating Potential	$R_{EB} = 10K$, $V_{CB} = -60v$ $-80v$	V_{EBF}		−0.1	−0.3 −0.5	Vdc
Emitter Junction Leakage Current	$I_C = 0$, $V_{EB} = -2v$ $= -28v$	I_{EBO}		−0.03 −0.15	−0.15 −2.0	mAdc
Collector Saturation Voltage	$I_C = -2a$, $I_B = -200ma$	$V_{CE}(sat)$		−0.15	−0.6	Vdc
Gain Bandwidth Product ($\sim f_{\alpha co}$)	$I_C = -100ma$, $V_{CE} = -4v$ $I_b = -1ma$	$h_{fe} \cdot h_{hfe}$	200			kc

*Applies to 2N539A only.

† Also available: JAN 2N539 and JAN 539A, processed to MIL-S-19500/38B

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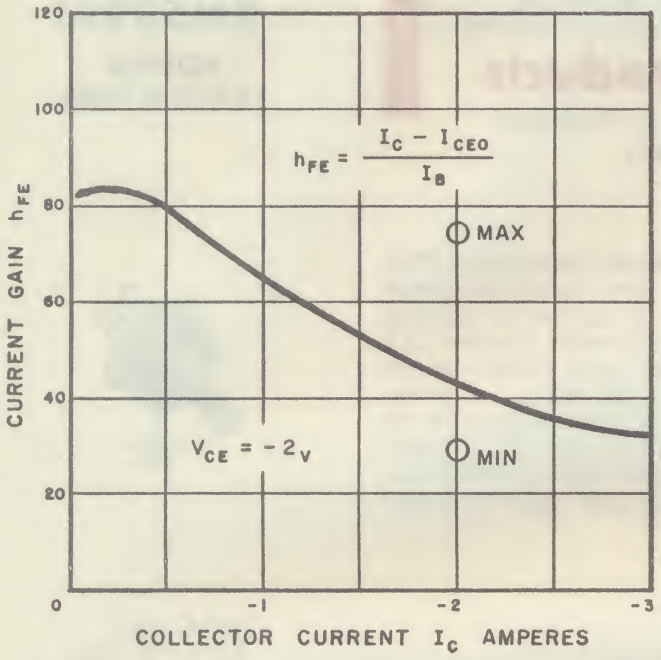
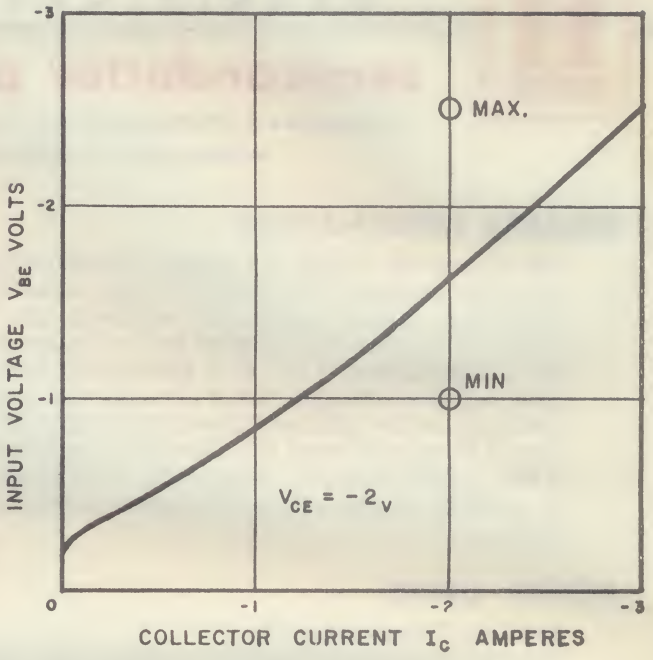
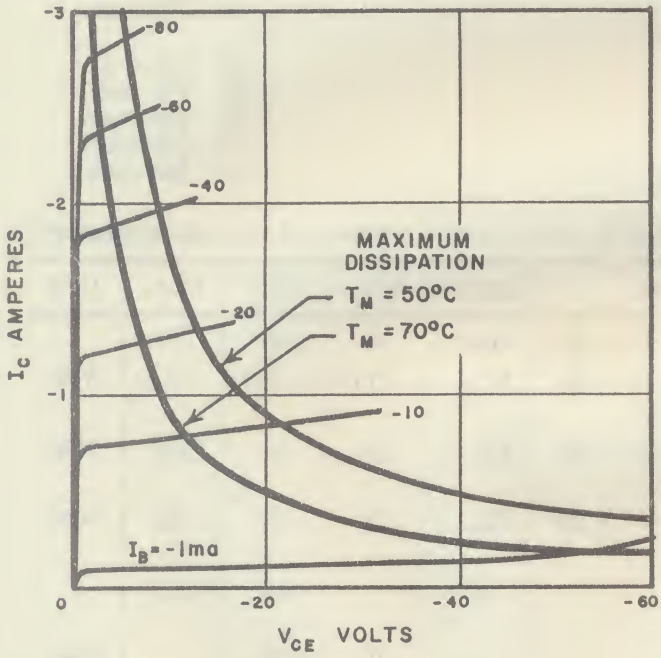
TYPICAL CHARACTERISTICS, $T_{MB} = 25^\circ$ C.

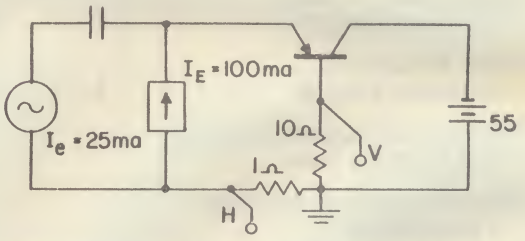






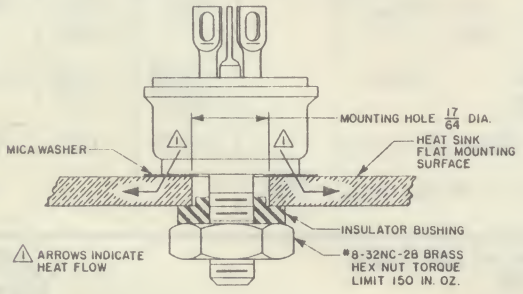
ALPHA = 1 VOLTAGE TEST

The voltage limit of a transistor in the active region is determined by the voltage at which $\alpha = 1$. The normal α, being less than unity, results in a current flow out of the base, and therefore a negative slope on an oscilloscope connected as shown in the circuit below. If the collector voltage is such that $\alpha = 1$, I_b will be zero and the slope of the oscilloscope trace will also be zero. If the voltage is such that $\alpha > 1$, the base current will reverse resulting in a positive slope of the trace.

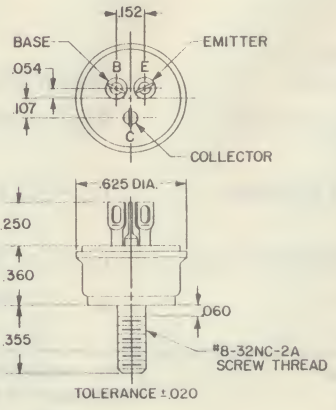


MOUNTING

It is very important that a power transistor be provided with a good heat dissipating facility. The surface to which the transistor is attached must be flat and free from burrs. The nut must be tightened securely (150 inch-ounce torque limit when used against a metal chassis or the bushing supplied, provided that all parts are clean and dry).



DIMENSIONS AND CONNECTIONS



These dimensions fulfill the requirements of the Registered EIA Transistor case TO-10 except for the 10-32-2A screw thread.

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